ACCESSING IN PARALLEL STORED DATA FOR ADDRESS TRANSLATION

Abstract of the Disclosure

A circuit to translate virtual addresses of varied page sizes into physical addresses enables selective access to an internally stored data in parallel to reading a specific physical address based on the input virtual address before the internally stored data matches in entirety for the address translation thereof. In one embodiment, a content addressed buffer may comprise at least two register files or static random access memories. For example, a banked architecture for a set associative translation lookaside buffer may reduce power consumption without compromising address translation speed.